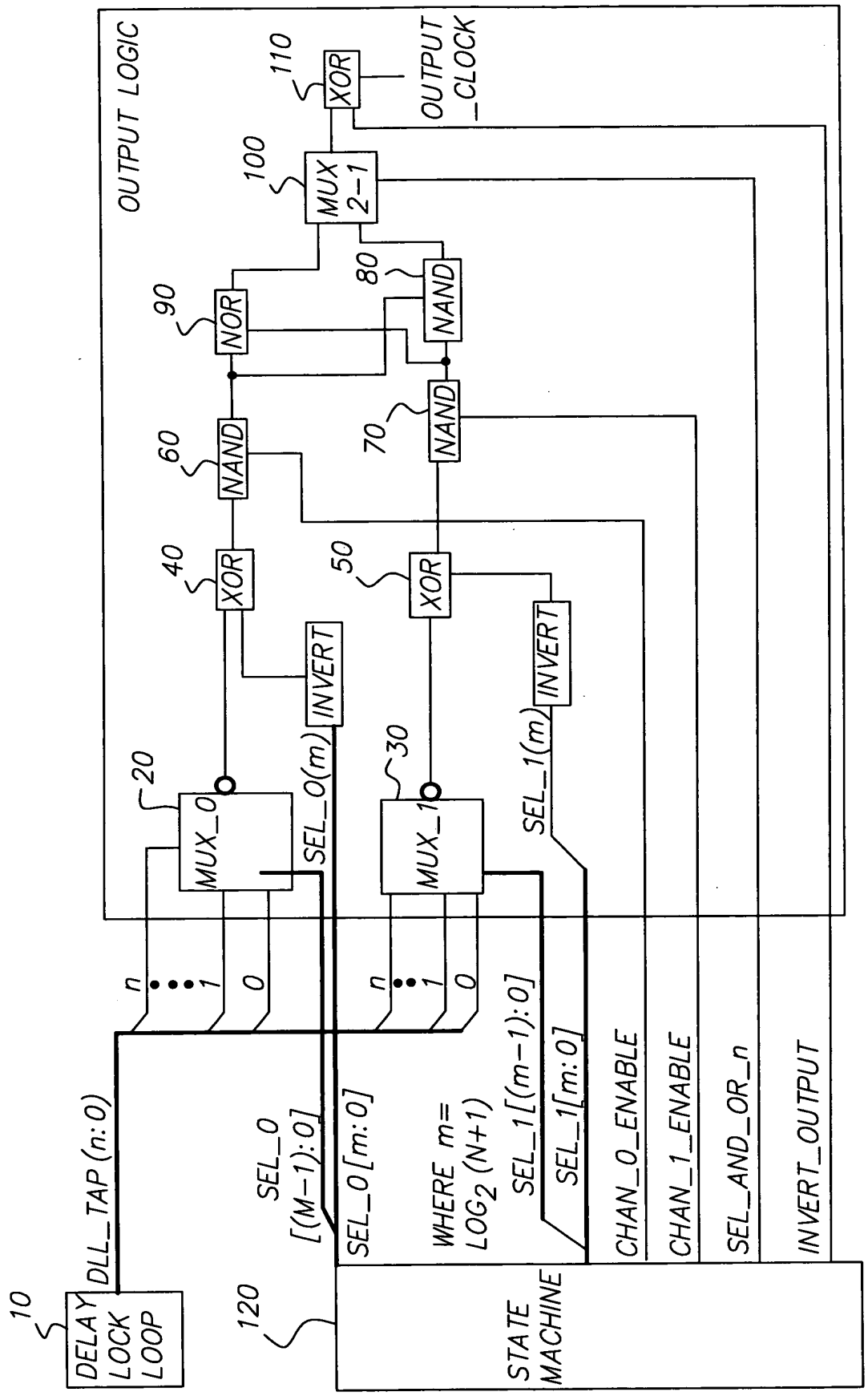

FIG. 1

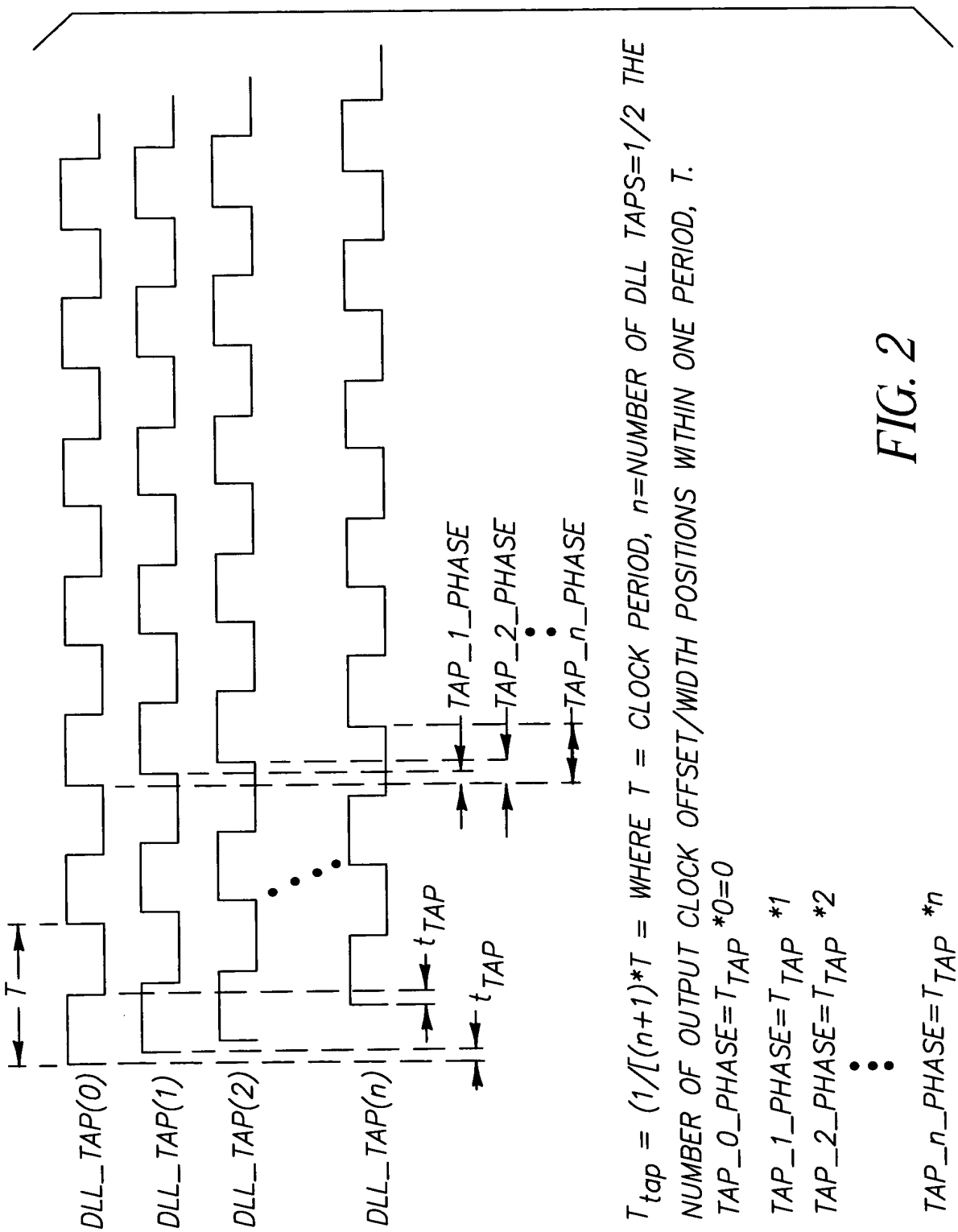
T
DLL_TAP(0)
DLL_TAP(1)
DLL_TAP(2)
DLL_TAP(n)
t TAP
t TAP
TAP_1_PHASE
TAP_2_PHASE
TAP_n_PHASE
T tap = (1/[(n+1)*T = WHERE T = CLOCK PERIOD, n=NUMBER OF DLL TAPS=1/2 THE NUMBER OF OUTPUT CLOCK OFFSET/WIDTH POSITIONS WITHIN ONE PERIOD, T.
TAP_0_PHASE=T TAP *0=0
TAP_1_PHASE=T TAP *1
TAP_2_PHASE=T TAP *2
TAP_n_PHASE=T TAP *n

FIG. 2

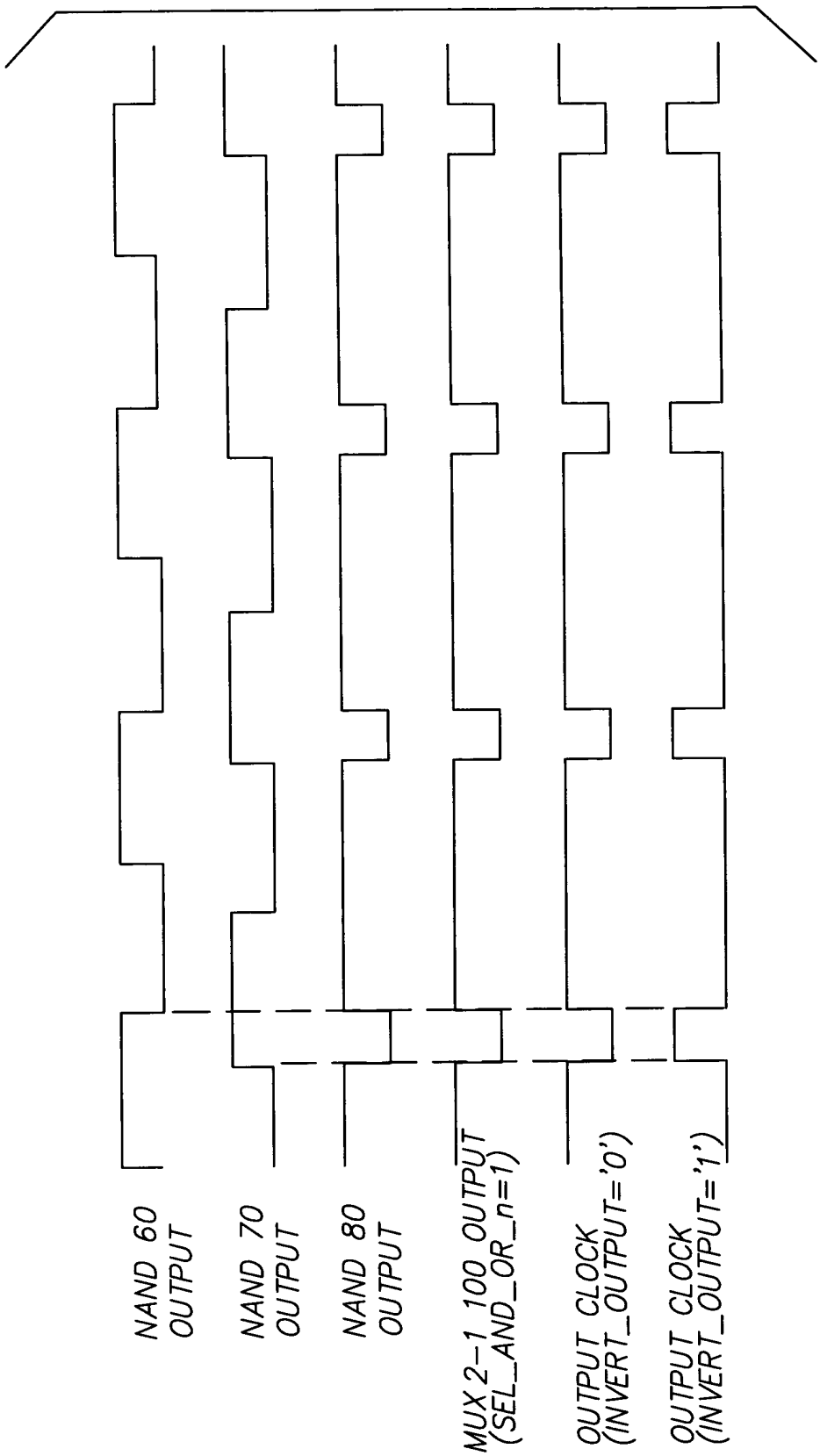
NAND 60 OUTPUT
NAND 70 OUTPUT
NAND 80 OUTPUT
MUX 2–1 100 OUTPUT (SEL_AND_OR_n=1)
OUTPUT CLOCK (INVERT_OUTPUT='0')
OUTPUT CLOCK (INVERT_OUTPUT='1')

FIG. 3

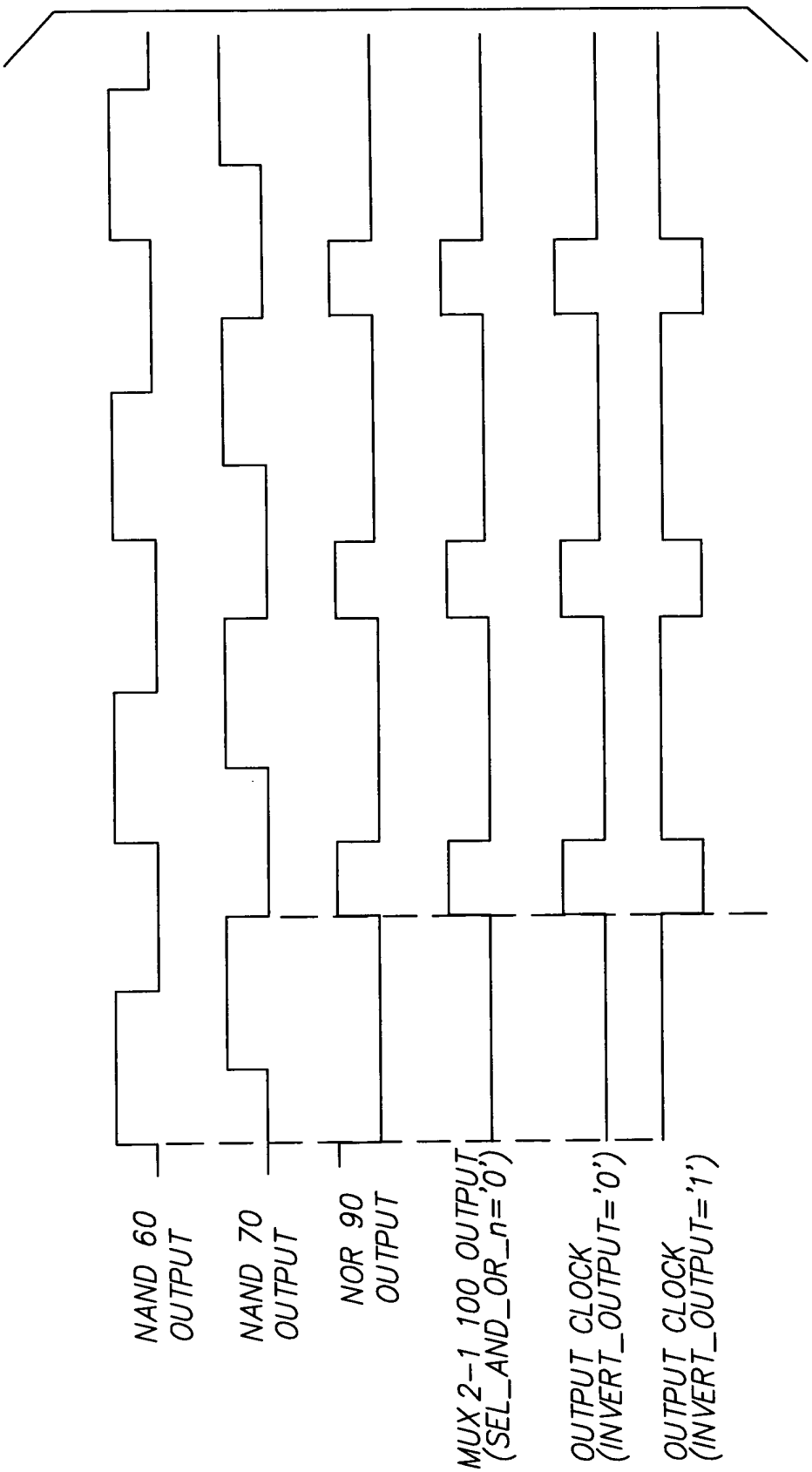
NAND 60 OUTPUT
NAND 70 OUTPUT
NOR 90 OUTPUT
MUX 2-1 100 OUTPUT ('SEL_AND_OR_n='0')
OUTPUT CLOCK ('INVERT_OUTPUT='0')
OUTPUT CLOCK ('INVERT_OUTPUT='1')

FIG. 4